DEPARTMENT OF DEFENSE

DEVELOPING SCIENCE AND TECHNOLOGIES LIST

SECTION 8: ELECTRONICS TECHNOLOGY

October 2000

Defense Threat Reduction Agency
Ft. Belvoir

PREFACE

The Developing Science and Technologies List (DSTL) is a product of the Militarily Critical Technologies Program (MCTP) process. This process provides a systematic, ongoing assessment and analysis of a wide spectrum of technologies of potential interest to the Department of Defense. The DSTL focuses on worldwide government and commercial scientific and technological capabilities that have the potential to significantly enhance or degrade US military capabilities in the future. It includes new and enabling technologies as well as those that can be retrofitted and integrated because of technological advances. It assigns values and parameters to the technologies and covers the worldwide technology spectrum.

The DSTL is oriented towards advanced research and development including science and technology. It is developed to be a reference for international cooperative technology programs. S&T includes basic research, applied research and advanced technology development.

SECTION 8—ELECTRONICS TECHNOLOGY

Scope

Highlights

- Moore's Law, which states that the number of transistors per chip will double every 18 months, continues to drive the electronic evolution and will enable smaller size, lower power, higher reliability, and lower cost electronics. However, the electronic materials and manufacturing technologies must be advanced to allow this rapid progress to take place, and this advance will be very costly.
- Nanoelectronics (below 100 nm) will be the successor to microelectronics but will require much research and development (R&D) in all areas since a paradigm shift in physics, materials, and processing is required.
- Microwave and other radio frequency (RF) components continue to progress, with increased power and frequency capability and reduced size and weight.

OVERVIEW

This section discusses the general-purpose integrated circuit (GPIC) devices and the materials and processes, software, test, and packaging technologies required to produce the finished product. These circuits can be digital, analog, hybrid digital and analog, analog-to-digital (A/D), and digital-to-analog (D/A) converters, microwave, and optical and optoelectronic if integrated on a GPIC or a module (see subsection 11.5 for optoelectronics).

Also included are:

- General-purpose modules made of these devices if packaged as multi-chip modules (MCMs) or printed circuit boards (PCBs)
- Other combinations of optical, microelectromechanical systems (MEMS), or micromachines used as sensors, effectors, input, output, or internal processing functions resulting in a "system-on-a-chip"
- Microwave components, vacuum tubes [e.g., traveling wave tubes (TWTs)] and their constituent parts
- General-purpose electronic equipment (e.g., test equipment, tape recorders, and their media and other general-purpose structures).

The electronic materials and fabrication technologies covered are unique to electronic manufacture and generally operate at the submicron dimension for electronics. One exception is the MEMS area, which produces devices at the multiple micro to submicron dimension using the same technology described in this section and which can be integrated into devices containing MEMS, electronic, and optical technologies. Other machine technologies can be found in Developing Critical Technologies Section 12, Manufacturing and Fabrication Technology.

The general trend of these technologies is to create rapidly the higher performance, smaller size, lower power, higher reliability, and greater integrated functionality necessary to perform a wide range of applications. The use of these products is pervasive across all applications, both commercial and military. The commercial sector is the primary driver and market for these products. However, the military sector has the same requirements for high performance, small size, lower power, and integrated functionality and has a greater requirement for reliability,

temperature range, and radiation-hardened (rad-hard) characteristics. The technologies involved in these products result in increasingly higher reliability and rad-tolerant devices because of the materials and processes involved.

The major force driving the electronics technologies is the goal of increasing the density of devices, with improvements in all the other characteristics noted previously and generally adhering to "Moore's Law," which anticipates halving device size every 3 years. For instance, the goal stated in the Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) for the year 2000 is 250–150 nm for production chips. These dimensions are pushing the present optical lithography technologies to their limit. Extreme ultraviolet (EUV) lithography will help continue the reduction in feature size (see subsection 8.3). However, attaining the next two generation goals of reduction to less than 100 nm will require a new paradigm of electronic technologies where Moore's Law may not apply. The new physics and the new fabrication processes necessary to reach this "nanoelectronic" capability are a huge challenge for the next century (see subsection 8.5).

As noted, commercial industry is the driving force for many advances in electronics technology—pushing lightweight, smaller size, and lower power devices as far as possible for laptop computers, handheld devices, and so forth. However, the military has the same goals for "personal wearable electronics," land-vehicle electronics, ultralightweight and unmanned surveillance aircraft for "the battlefield of the future," ocean applications (e.g., smart mines), and space electronics. Many of these military applications require even lower power, smaller size, and higher reliability than any commercial application.

SECTION 8.1—ELECTRONIC COMPONENTS/MICROWAVE TUBES

Highlights

- Microwave power modules (MPMs) offer increased power and frequency capability, with reduced size and weight.
- Improved cathodes with lower work functions will result in microwave tubes that can operate with greater efficiency, higher current density, and longer cathode life.
- Overall improvements in TWT technology will result in TWTs capable of operating in the kW power range, at frequencies greater than 90 GHz.

OVERVIEW

This subsection addresses developing technologies in the field of high-power microwave components, with particular application in surveillance, satellite communications, electronic warfare (EW), missile seekers, and tracking radar. These modern weapons require high levels of microwave power, and semiconductors are presently not suitable for these high-power applications. Although development of SiC semiconductor devices may alleviate this shortcoming, microwave tubes are presently the most effective devices for these applications.

Efforts to enhance the performance of these microwave components include improving each of the inherent parts of conventional TWTs (including the cathode), improving the cooling of the RF section (particularly in helix tubes), improving the ability of the electron beam to focus, and combining the technologies of TWTs with solid-state devices to form assemblies called MPMs. Research to improve the cathodes includes efforts on thermionic and nonthermionic cathodes, specifically developing new coating materials to extend the life of the cathodes and their current densities and evaluating the use of field-emission cathode arrays (cold cathodes). Improved cooling of the TWT has a significant effect on the power handling of the tube, and studies are being performed on the effect of substituting diamond-coated rods, with their superior thermal conductivity, for the more conventional support rods used in helix tubes. Focusing is a critical aspect of tube design and manufacture since energy that falls on (is absorbed by) the RF structure decreases the efficiency of the tube. Studies are also underway to develop stronger and more reliable magnets to minimize the "stray energy," thus improving the efficiency of the TWTs.

MPMs combine several technologies: mmW integrated circuits (MMICs) for amplification, helix TWTs for power amplification, and an electronic power conditioner (EPC). This combination of technologies provides optimum use of each of the technologies: frequency amplification by the MMICs and power amplification by the TWTs.

LIST OF TECHNOLOGY DATA SHEETS
8.1. ELECTRONIC COMPONENTS/MICROWAVE TUBES

DATA SHEET 8.1. GYROTRON OSCILLATOR AND GYRO-AMPLIFIER

Developing Critical Technology Parameter	Continuous wave (CW) power greater than 5 MW and a frequency greater than 30 GHz.
Critical Materials	Superconducting coils; exit window material.
Unique Test, Production, Inspection Equipment	None identified.
Unique Software	None identified.
Major Commercial Applications	Fusion research; thermal processing of materials (ceramic sintering and welding); driving linear colliders.
Affordability	Not an issue.

BACKGROUND

Gyrotron oscillators have opened up the mmW region (1-to-10 mm) for high-power applications. Present gyro-devices are capable of operating at continuous power levels approaching 1 MW at frequencies exceeding 100 GHz. Present gyro-amplifiers (e.g., gyro-klystrons) are capable of operating at average power levels of 10 kW over a 1-GHz bandwidth at a center frequency of 94 GHz. Military applications are mmW radar (e.g., fire control radar and tracking radar for targets close to the sea surface).

DATA SHEET 8.1. IMPROVED CATHODES: FIELD-EMISSION CATHODE ARRAYS (COLD CATHODES)

Developing Critical Technology Parameter	Current densities of 1,000 –2,000 A/cm^2.
Critical Materials	Silicon; diamond (carbon); GaN; other materials being researched to form field emission tips.
Unique Test, Production, Inspection Equipment	Photolithographic equipment; plasma etchers; and so forth.
Unique Software	Computer-aided design/computer-aided manufacturing (CAD/CAM).
Major Commercial Applications	Space electronics; radar systems; flat panel displays (FPDs).
Affordability	Not an issue.

BACKGROUND

Field-emission cathode arrays hold great promise for improving microwave devices. They should provide much greater current densities (and, thus, greater output power) than more conventional heated cathodes and do not require external heaters. Thus, TWTs using this type of cathode could not only produce greater power, but, because of the absence of heaters, produce this power in a smaller device envelope.

DATA SHEET 8.1. IMPROVED CATHODES: OXIDE-COATED CATHODES

Developing Critical Technology Parameter	Reduce work function from 2.0 eV–1.2 eV.
Critical Materials	Oxide-coated cathodes: barium and strontium oxides, scandate (Sc_2O_3); indium and scandium oxides; and indium as an additive; impregnated cathodes; lanthium hexaboride cathodes.
Unique Test, Production, Inspection Equipment	Deposition techniques (usually plasma deposition); pulsed laser deposition.
Unique Software	None identified.
Major Commercial Applications	Space electronics and radar systems.
Affordability	Not an issue.

BACKGROUND

By developing cathodes with lower work functions, microwave tubes can operate with greater efficiency (i.e., greater output power at the same level of dissipated heat) and higher current density and enjoy longer cathode life. These improvements would be of value for a range of microwave tubes, TWTs, magnetrons, and so forth.

DATA SHEET 8.1. IMPROVED COOLING OF HELIX TUBES

Developing Critical Technology Parameter	Increase in thermal conductivity by a factor of 5–10; a reduction in the coefficient of thermal expansion by a factor of 2–3.
Critical Materials	Diamond-coated components; high thermal conductivity ceramics.
Unique Test, Production, Inspection Equipment	Chemical vapor deposition (CVD) equipment for the deposition of diamond films.
Unique Software	None identified.
Major Commercial Applications	Space electronics and radar systems.
Affordability	Not an issue.

BACKGROUND

All mmW components generate heat, and the dissipation of this heat is important for the proper operation of the components. Continued improvements in these devices will depend, along with other developments, on improved methods to dissipate heat.

DATA SHEET 8.1. MILLIMETER-WAVE (mmW) TRAVELING WAVE TUBES (TWTs)

Developing Critical Technology Parameter	Frequency > 90 GHz; output power ≥ 200 W; weight < 20 kg.
Critical Materials	Scandate (Sc_2O_3) cathodes; diamond-coated rods; Samarium Cobalt magnets; high thermal conductivity ceramics.
Unique Test, Production, Inspection Equipment	Machine (including micromachines) tools to manufacture the TWT components.
Unique Software	CAD/CAM.
Major Commercial Applications	Space electronics; radar systems.
Affordability	Not an issue.

BACKGROUND

TWTs are essential components in radar, EW, countermeasures, missile electronics, UAVs, communications, and space applications. Research is being conducted to address the following characteristics: broad bandwidth, high efficiency, high gain, high voltage stand-off capability, low noise, compact size, low weight, lower cost, and improved reliability.

DATA SHEET 8.1. MICROWAVE POWER MODULES (MPMs)

Developing Critical Technology Parameter	Power greater than 1.5 kW in X-band; power greater than 1 kW in I/J-band; efficiencies greater than 50 percent; size/weight less than one-fifth of conventional TWTs.
Critical Materials	Silicon or gallium arsenide for the integrated circuits (ICs).
Unique Test, Production, Inspection Equipment	Standard equipment for the manufacture of ICs; machine tools for the manufacture of the TWT components.
Unique Software	CAD/CAM.
Major Commercial Applications	Space electronics and radar systems.
Affordability	Not an issue.

BACKGROUND

The MPM is capable of providing high power over wide bandwidths at high efficiency. It is also smaller and less expensive than conventional TWTs.

MPMs include three basic parts: a vacuum power booster (VPB) (a helix TWT), a solid-state amplifier (SSA) (an MMIC), and an EPC. The EPC converts the input voltage to the proper operating voltages for the VPB and the SSA and monitors the condition of the module. The SSA receives the RF input, amplifies it, and provides the RF drive to the VPB. The VPB provides the high-power RF output.

SECTION 8.2—ELECTRONIC MATERIALS

Highlights

- Separation by the Implantation of Oxygen (SIMOX) silicon-on-insulator (SOI), made by high-energy implantation of oxygen into a heated silicon substrate, results in a thin layer of silicon separated from the substrate by an insulating layer of silicon dioxide.
- SiC-based electronics and sensors can operate in hostile environments where conventional silicon-based electronics (limited to 350 ℃) cannot function.

OVERVIEW

This technology area includes preparing and processing new and current electronic materials from the purification of the basic elements to the final wafer or substrate material ready for device fabrication. Materials handling and their processes are currently undergoing rapid changes to meet the future demands of the electronic industry. These materials are made of very pure starting materials.

Depending on the material under consideration, preparation methods are numerous, including SIMOX made by high-energy implantation of oxygen into a heated silicon substrate. SIMOX wafers are created by implanting oxygen atoms below the surface of a silicon wafer in sufficient quantity to transform the silicon-to-silicon dioxide. After implantation, the wafers are carefully annealed at high temperatures, typically 1,325 °C, to repair defects introduced by the oxygen implantation and to crystallize the silicon dioxide. The insulating silicon dioxide separates the top silicon layer from the substrate, and ICs are then fabricated in the top silicon layer. A second method used to form SOI uses ion implantation and wafer bonding technologies. Starting with two wafers, the silicon surface of one wafer is first oxidized to form what will become the buried oxide layer of the SOI structure. An ion implantation step, using hydrogen ions, is then executed through the oxide layer by a standard high-current ion implanter to form a usable thin layer of silicon and a layer of microbubbles at the path length of the hydrogen implant. The second wafer is then bonded to the oxide layer. The sandwiched wafers are thermally treated and break apart at the microbubble layer, which is then annealed and polished. The surface silicon of the finished wafer has very low defect levels that approach those in bulk silicon. The oxide layer is pinhole free.

The successful growth of heteroepitaxial SiC with high resistivities and low-defect densities, improved epilayer doping, and thickness control on large area substrate materials [greater than 3 in. using metallo organic chemical vapor deposition (MOCVD)] and epitaxial growth equipment are critical to military electronics.

LIST OF TECHNOLOGY DATA SHEETS
8.2. ELECTRONIC MATERIALS

DATA SHEET 8.2. SILICON CARBIDE (SiC)

Developing Critical Technology Parameter	SiC-based electronics and sensors can operate in hostile environments where conventional silicon-based electronics (limited to 350 °C) cannot function. The performance of these devices is severely degraded at elevated temperatures, at the highest RF powers, and in harsh radiation conditions. SiC's ability to function in high-temperature, high-power, high-frequency, and high radiation conditions will enable large performance improvements to a wide variety of military systems and applications. These include solar blind detectors; microwave/millimeter radar; communication; EW and missile seeker systems; high-current, high-voltage; and high-speed requirements of CW and pulsed electrical subsystems in emerging hybrid-electric and all-electric combat vehicles, more electric airplanes, and naval ships. Research is focused on developing the base crystal growth and device fabrication technologies necessary to produce a family of SiC high-temperature, high-power electronic devices and circuits to meet system demands for hostile environment.
Critical Materials	SiC bulk crystals; thin films of epitaxial-grown SiC.
Unique Test, Production, Inspection Equipment	MOCVD; epitaxial growth equipment; bulk and surface lifetimes measuring systems for ultrathin films; spectroscopic ellipsometer; spectrophotometer; defect detection and classification equipment; interferometeric measurement equipment.
Unique Software	Special algorithms to control the growth process of the materials; metrology equipment software.
Major Commercial Applications	Capability of operation in the 600 °C region at power levels of 1,000 V and current densities exceeding 1,000 Å/cm^2 provides electronic devices and circuits to meet system demands for hostile-environment electronics. In addition, solid-state electronics have to improve the transmission, distribution, and quality of electric power in the utilities Industry.
Affordability	In addition to substrate price, the development of an inexpensive epitaxial process for SiC is a major precondition for manufacturing SiC devices at a lower cost.

BACKGROUND

Conventional semiconductor electron devices, such as field-effect transistors (FETs), are fabricated using silicon or compound semiconductors, such as GaAs. The performance of these devices is severely degraded at elevated temperatures and in harsh environments where harmful radiation may be present.

In the last decade, a concerted worldwide effort has emerged to develop the next generation of electronic devices that would be able to operate at elevated temperatures and in harsh environments (e.g., outer space). Such devices would be fabricated using semiconductor materials that have a large bandgap [more than 2 eV (i.e., about twice that of conventional semiconductors such as silicon and GaAs)]. Examples include SiC and diamond. Unlike silicon, SiC-based devices can operate reliably in environments in excess of 150 °C and are capable of operation in the 600 °C region. The use of SiC eliminates the need for remote cabling or cooling systems by enabling devices to function in the hot areas of high-speed airframes, aircraft, and internal combustion engines and in other macro devices, platforms, and systems that operate at temperatures in excess of 400 °C. In the field of power electronics, SiC distinguishes itself as being capable of handling several thousand volts in reverse mode and at least 1,000 Å/cm^2 in forward mode for use in high-power switches operating at 1,000 V and at current densities exceeding 1,000 Å/cm^2. Specific issues that need to be resolved include suitable "substrate" for epitaxial growth, suitable dopants for p- and n-type materials, reduction of dislocations that arise in epitaxial layers because of differences in the lattice constants and in coefficients of thermal conductivity, and the ability to grow materials over large wafer areas.

DATA SHEET 8.2. SILICON-ON-INSULATOR (SOI) SEPARATION BY THE IMPLANTATION OF OXYGEN (SIMOX)

Developing Critical Technology Parameter	More precise, high-energy oxygen implantation technology for the production of 200–300 mm-diameter wafers with thin single crystal silicon (less than 1000 Å) and oxide insulating layer (less than 300 Å by the year 2006) wafers (see ***Background***).
Critical Materials	Large area (200–300 mm) silicon wafers.
Unique Test, Production, Inspection Equipment	High-energy (250 keV) oxygen and low-energy (100 keV) hydrogen implanters; atomic absorption; X-ray reflective measuring equipment.
Unique Software	Ion implantation beam; metrology; diagnostic software.
Major Commercial Applications	Low-power, high-speed, and high-temperature applications (see ***Background***).
Affordability	Cost of SOI wafers is basically twice the cost of bulk silicon. The primary benefit commercializing SOI will be the reduced starting material costs and the producibility of SOI starting material.

BACKGROUND

SiO_2 films play a central role in semiconductor technology. $SiO_2$is used as a very thin film separating the gate electrode and the Si substrate in complementary metal-oxide semiconductor field-effect transistors (CMOS FETs). The CMOS FET is an essential device for most ICs, including gate arrays, microprocessors, dynamic random access memory (DRAM), flash memories, silicon-on-chip system ICs, and so forth. The SiO_2 film's resistance against degradation is crucial to the reliability of the CMOS-FETs and, hence, to the IC chips themselves. The thickness of the film is an important parameter in determining the performance (signal speed) and level of integration. To reach the level of 4 Gbits/chip DRAM integration and performance level, the SiO_2 thickness must be scaled down from its present thickness of 3.5 nm to a thickness of approximately 2 nm.

Advantages of SOI technology include high speed, size reduction, and increased temperature range. Advanced gigahertz-level microprocessors are capable of surviving high radiation dose rates. The SIA NTRS estimates that IC manufactures will continue to use SiO_2 as gate-dielectric material up to the 4 Gbits/chip DRAM level. New materials are expected to replace SiO_2 above that level.

High-energy implantation of oxygen into a heated substrate of silicon is known as SIMOX. Standard SIMOX wafers are created by implanting oxygen atoms below the surface of a silicon wafer in sufficient quantity to transform the silicon to SiO_2, while maintaining a thin surface layer of circuit-quality, single-crystal silicon. After implantation, the wafers are carefully annealed to repair defects introduced by the oxygen implantation and to crystallize the SiO_2. The insulating SiO_2 separates the top silicon layer from the substrate, and ICs are then built in the top silicon layer.

High-temperature space applications are a concern. Thermal shielding for satellites is quite heavy, and the weight of a satellite has a direct impact on the cost of placing it in orbit. In some special applications (Venus probes), shielding is no longer possible, and high-temperature electronics are absolutely required. Much higher temperature tolerance is required from engine-monitoring electronics, such as electronic injection systems, where precision control of the injector position is controlled by electronic components located close to or within the engine block. Modern antilock braking systems (ABSs) also require electronic control systems placed close to the brakes, and these systems are exposed to high temperatures when the brakes are activated. The ability of SOI CMOS to operate at high temperatures, combined with the possibility of integrating power devices with low-power logic on a single, dielectrically isolated substrate, renders SIMOX the ideal technology for such purposes. High-temperature airplane applications include onboard electronics and, of course, engine control and surface control (wing temperature).

The production of UNIBOND® wafers uses both ion implantation and wafer bonding technologies. Starting with two wafers, the silicon surface of one wafer is first oxidized to form what will become the buried oxide layer of the SOI structure. An ion implantation step using hydrogen ions is then executed through the oxide layer by a standard high-current ion implanter to form a usable thin layer of silicon and a layer of microbubbles at the path length of the hydrogen implant. The second wafer is then bonded to the oxide layer. The sandwiched wafers are thermally treated and break apart at the microbubble layer, which is then annealed and polished. The surface silicon of the finished wafer has very low defect levels that approach those in bulk silicon. The oxide layer is pinhole free. The remaining wafer, which is still within Semiconductor Equipment and Materials International (SEMI) standards for thickness specifications, is reclaimed and polished. It is then used as the support wafer for producing the next UNIBOND® wafer.

This SOI UNIBOND® technology solves the two limitations of conventional bonding. The uniformity for thin SOI layers is obtained because ion implantation is used, and, since the second wafer is saved, the traditional wafer-bonding cost barrier caused by the consumption of two starting wafers to produce one SOI wafer is eliminated.

SECTION 8.3—ELECTRONIC FABRICATION

Highlights

- Lithographic technologies use 193-nm ultraviolet (UV) lithography and EUV lithography (EUVL) for fabrication devices with line widths of 100 nm.
- Lithographic technologies use proximity X-ray, electron beam (e-beam) projection, electron-beam direct write (EBDW), and ion projection for the fabrication of semiconductor devices.
- Lithographic technologies can generate and transfer highly complex patterns for MEMS.
- Nanotechnology provides the capability to design, fabricate, and test electronic devices with critical feature sizes below 0.1 μm.
- MEMS technology enables the development of chemical, biological, and mechanical smart systems.
- Specially designed semiconductor processing modules provide a unique integrated system for sequential multiple processing of wafers in a vacuum environment.

OVERVIEW

This subsection addresses the developing semiconductor processing equipment technologies used to fabricate devices for military systems. (The same process is used in commercial fabrication.) The technologies will either provide a superior final device or reduce the cost of fabricating the existing device. These technologies involve the growth of epitaxial layers, implantation of dopants, the use of cluster tools for the deposition and etching of thin-film layers, single-wafer processing, delineation of patterns using lithographic techniques, and testing and packaging of ICs. They are also used for passive and active devices, MEMS, and sensors in military equipment and systems.

Optical lithography continues to be the mainstream technology for the semiconductor industry and is being used in production at 250-nm design rules. Extensions of optical technology are being used to support 180-nm product and process development. Advanced technologies, such as X-ray and EBDW, have been used to fabricate functional semiconductor devices below 100 nm over small field sizes at low throughput. In addition, various technologies have been proposed, and studies are underway for resolution capability down to 50 nm.

One promising technology that builds on the optical experience is EUVL using 10- to 14-nm soft X-ray photons; however, overlay and critical dimension (CD) improvements have not kept pace with resolution improvements. The estimates for overlay appear to plateau around 30 nm. This will be inadequate for ground rules less than 100 nm. Overlay and CD control over large field sizes will continue to be a major concern for < 130-nm lithography. Continuous improvements in mask-making technology (mask writers, inspection, repair, and substrates) continue to be required to support the technical and manufacturing needs of optical lithography below 250 nm.

MEMS include sensors and actuators that are fabricated using IC production processes. Automotive, biomedical, aerospace, and robotic MEMS devices are produced with combinations of bulk and surface micromachining. MEMS processing uses these technologies to create structural components that are essentially submillimeter-sized machine parts. High-energy oxygen implanters are used to produce SOI wafers—a technology that has long been relegated to radiation-hardened circuits for military and space environments, a small niche market. Ion implanters to be used in fabricating large-area SOI wafers for the development of gigahertz-level microprocessors are being developed. SOI would offer a 20- to 35-percent performance improvement because of reduced capacitance, a by-product of having a thin oxide layer under the transistors.

LIST OF TECHNOLOGY DATA SHEETS
8.3. ELECTRONIC FABRICATION

DATA SHEET 8.3. CLUSTER TOOLS

Developing Critical Technology Parameter	Cluster tools will enable an extensive set of sub-0.15 µm gate, capacitor, and shallow trench isolation applications, with excellent CD control, operational flexibility, and damage-free results for sub-0.15 µm device designs with sub-20Å gate oxides. Cluster tools' superior degree of process control offers high-etch-rate in situ process integration capability, near vertical profiles, high selectivity of substrates, and excellent repeatability of results. The tools' new controllable magnetic field technology and advanced temperature control will provide uniform, damage-free results over an extremely broad operating window. The systems' advanced and emerging interconnect technology (in situ damascene integration, main dielectric etch/PR and polymer removal/nitride barrier removal, copper interconnects, low-k dielectrics, and advanced contacts) provides chip makers with next-generation 0.10-µm extendibility that delivers high throughput, enhanced reliability, and the flexibility to deliver advanced applications for new and emerging interconnect technologies. In addition, upgrades and retrofits are available for existing tools to facilitate the deposition and etch solutions needed for 0.15 µm, 0.10 µm, and beyond.
Critical Materials	Surface finish of metal components, hardness, and chemical inertness; outgassing properties; dimensional stability.
Unique Test, Production, Inspection Equipment	Real-time closed loop in situ automated process control; defect detection and classification; wafer tracking and transport; communication standardization.
Unique Software	Specially designed algorithms for process control.
Major Commercial Applications	For the semiconductor industry, integrated processing was the newest technology driver of the 1990s, and cluster tools became the vehicles for implementing the concept. In the next few years, more and more IC processes will be implemented in cluster systems—not only for the most often-cited reasons (contamination control, yield improvement, throughput, and so forth) but also because of increasing competitive pressure on the world's semiconductor manufacturers for improved, economically efficient manufacturing.
Affordability	The cost of cluster tools is very high. They remain a major precondition for manufacturing state-of-the-art ICs.

BACKGROUND

Cluster tools are semiconductor fabrication processing systems that have some of the following unique features: a stored program, controlled, automatic loading central wafer handling system; specially designed interfaces for wafer input and output; specially designed semiconductor processing modules or chambers capable of doing process steps such as epitaxial growth, CVD, physical vapor deposition (PVD), etch, oxide growth, passivation, and anneal; a communication system that provides an integrated system for sequential multiple processing of wafers in a vacuum environment; single wafer and sequential multiwafer processing; and sequential batch processing. Cluster tools can be divided into two areas:

- A highly sophisticated system that provides an integrated system for sequential multiple processing of wafers
- A system that does batch processing where one processing step (i.e., deposition or etch) takes place in a highly controlled environment.

The evolution of cluster tools has progressed from the addition of load locks and process systems, to load lock, preclean, process, and passivation, to the integration of more than one process step in the same system. Cluster tools can be used for plasma-enhanced CVD, dry etch, high-pressure oxidation, rapid thermal anneal, and numerous other

processes either as a batch system performing one process or as a system performing sequential processing steps. Processes that could not be done using standalone systems can now be done using a cluster tool (e.g., the selective deposition of tungsten).

With an integrated process, one can first use an etch chemistry to remove any ambient-formed oxide and condition the silicon surface at the bottom of the plug (because tungsten does not adhere well to silicon oxide) and then immediately begin growing tungsten. Both steps can take place under vacuum and in rapid sequence, thus inhibiting the formation of oxide layers between films, which reduce selectivity and increase contact resistance.

In the near future, lithography clusters capable of robotically changing and aligning a reticle in less than 1 min will be in commercial production lines and will enable manufacturers to have wafers with different devices in the same batch. Because the days of commercial production lines dedicated to military circuits are coming to an end and military systems are using more COTS parts, the capability for low-volume production becomes very important. This capability serves the low-volume requirements of the military and the commercial sectors. With the transition to larger 300-mm wafer sizes, single wafer processing tools have become a requirement to maintain reliable process control. In these systems, multiple process modules, each independently processing individual wafers, cluster around a single wafer handler.

DATA SHEET 8.3. ENHANCED OPTICAL LITHOGRAPHY

Developing Critical Technology Parameter	Lithographic technologies for the generation and transfer of highly complex patterns for microelectronics and micromechanical structures using 157-nm UV lithography and EUVL employing 10–14-nm soft X-ray photons [see ***Background; Lithographic Requirements*** **(Table 8.3-1)**; ***Extreme Ultraviolet Lithography (EUVL)***].
Critical Materials	Advanced resist systems (bi-layer, thin-layer imaging, chemically amplified); optical materials; antireflective materials for optical; EUVL.
Unique Test, Production, Inspection Equipment	Optical, EUVL exposure equipment; phase shift masks; mask inspection equipment; wafer level defect recognition and analysis.
Unique Software	Defect recognition and analysis; OPC; statistical quality control (SQC).
Major Commercial Applications	Lithography is used in fabricating all semiconductor devices, ICs, and MEMS devices.
Affordability	Not an issue.

BACKGROUND

Lithography is the enabling technology that has supported the IC industry for decades. Lithography and micropattern transfer technology used to fabricate devices and ICs are the keys in determining their performance and maintaining a strategic edge in a wide range of military sensors, EW devices, communications, command and control (C2), and offensive and defense weapon systems. New, advanced lithographic technologies are required to adhere to the advanced performance projections for IC devices in the 21st century.

Lithographic Requirements

Optical lithography (nominally defined for wavelengths of 157 nm and greater) continues to be the mainstream technology for the semiconductor industry. It is about to enter in production at 180-nm CD design rules. Improvements to optical technology will be required to support product and process development at CDs of 180 nm and below. Resolution enhancement techniques (RETs) include wavelength reduction (193 nm–157 nm) and off-axis illumination, as well as PSM and OPC. The key challenge to optical enhancement at the 130-nm CD level will be maintaining an adequate and affordable process latitude (depth of focus/exposure window) necessary for 10-percent post-etch CD control. Mask-making capability exists for 250-nm generation chrome binary masks. Capability for complex PSM, OPC, and 180-nm binary masks are in development and pilot production. Solutions for rapidly growing data volumes need to be developed, especially for optical proximity correction in the < 250-nm regime. Advanced I-line resists are in manufacturing, with resolution capabilities down to 300 nm. DUV resists at 248 nm are commercially available and are being used to manufacture 64-MB DRAM and MPU products.

Overlay requirements are among the most difficult technical challenges in lithography. Overlay and CD improvements have not kept pace with resolution improvements. The estimates for overlay appear to plateau around 30 nm, which will be inadequate for ground rules less than 100 nm. Overlay CD control over large field sizes continues to be a major concern for < 130 nm lithography. Advances in stage technologies, environmental controls, interferometers, and alignment systems will be needed for < 65 nm overlay. Continuous improvements in mask-making technology (mask writers, inspection, repair, and substrates) are required to support the technical and manufacturing needs of optical lithography below 250 nm. Table 8.3-1 lists projected advances in lithography and overlay.

Mask inspection requirements will become more aggressive as optical lithography pushes to finer resolutions. Major process and materials development is required to achieve the tolerances and mechanical properties necessary in the unique substrates used in these advanced technologies. Key issues will be identifying and repairing defects and the ability to keep masks defect free in manufacturing.

Table 8.3-1. Critical Level Lithography Requirements
(Source: SIA NTRS)

Year of Production	1999	2001	2003	2006	2009	2012
Technology Generation	**180 nm**	**150 nm**	**130 nm**	**100 nm**	**70 nm**	**50 nm**
Product Application						
DRAM (bits)	1G	2G	4G	16G	64G	256G
MPU (logic transistors/cm^2)	6M	10M	18M	39M	84M	180M
ASIC (usable transistors/cm^2)	14M	16M	24M	40M	64M	100M
Minimum Feature Size						
MPU Gates (Isolated lines)	140	120	100	70	50	35
DRAM (Dense lines)	180	150	130	100	70	50
Contacts	200	170	140	110	80	60
Gates (nm, 3 sigma)	14	12	10	7	5	4
Overlay (nm, mean + 3 sigma)	65	55	45	35	25	20
DRAM Chip Size (mm^2)						
Year 1	400	480	560	790	1120	1580
Year 2	320	390	450	630	900	1300
Year 3	240	290	340	480	670	950
MPU Chip Size (mm^2)						
Year 1	360	400	430	520	620	750
Year 2	290	240	260	310	370	450
Year 3	220	240	260	310	370	450

Extreme Ultraviolet Lithography (EUVL)

Optical lithography has provided the enabling technology to support the IC industry for several decades. However, new approaches will be required to maintain the Moore's Law projections for IC manufacturing in the 21st century. One promising technology, which builds on the optical experience, is EUVL using 10–14 nm soft X-ray photons. For these wavelengths and 4× reduction, low numerical aperture (NA) imaging systems with printing resolutions less than 100 nm and a depth of focus (DOF) greater than 1 nm are expected. Technology scaling is expected to support several IC generations down to possibly 0.03 nm.

Because extreme ultraviolet (EUV) photons are highly absorbed in most materials and gases, special reflective optics contained in a vacuum environment are required to produce imaging.

The EUVLLC lithography goals include:

- An engineering test stand (ETS) in late 1999
- Stepper beta tools by 2001
- Pre-production and production tools by 2002 and 2004, respectively.

The initial lithography tool goals for the illuminator include using a continuous, recycling xenon gas jet laser plasma source and a 13.4-nm condenser delivering > 98-percent uniformity and < 2-percent nonuniformity illumination over a 1.5 × 26 mm ring field with a partial coherence of 0.7. The production lithography tool targets a scanned field the size of 26 mm × 52.5 mm printed on 300-mm wafers using 150-mm and 300-mm reflective masks and 4:1 reflective reduction projection optics. Wafer and reticle-handling interfaces will support a 300-mm system in a contamination-free vacuum environment with a throughput of 40 wafers per hour.

DATA SHEET 8.3. NANOTECHNOLOGY

Developing Critical Technology Parameter	Develop material, processing technologies, < 100-nm lithography, quantum and conventional devices, and device architectures for a next generation of information processing systems and subsystems with critical feature sizes well below 0.1 µm. Improve speed, density, power, and functionality to achieve speeds 10 to 100 times faster than current systems, density by a factor of 5–100, and lower power by a factor of more than 50.
Critical Materials	Resist for 193-nm and soft X-ray lithography, elastomeric polydimethylsiloxane (PDMS) for soft lithographic replication.
Unique Test, Production, Inspection Equipment	Highly anisotropic reactive ion etching (RIE) system; scanned probe microscopies; atomic force microscope; nano-positioning devices; nanoprobes for diagnostics; auger spectroscopy; high-temperature X-ray; neutron-scattering techniques.
Unique Software	None identified.
Major Commercial Applications	For the manipulation of materials and data at the atomic level for applications such as computer storage technology, single electron tunneling (SET) devices are predominantly aimed at high-density, low-power memory markets. Resonant tunneling diodes (RTDs) have demonstrated numerous applications, and potential markets include digital-to-analog converters (DACs), clock quantisers, shift registers, and ultralow power SRAM. The RTDs can be designed for much higher speeds than CMOS for DACs and so forth, typically in the speed range 10 to 100 GHz, or for much lower power than CMOS, such as the SRAM technology. Phase shifter/frequency translator based on serrodyne modulation of a nonlinear transmission line for integrated sensor applications using terahertz signals.
Affordability	In reference to Moore's Law, manufacturers state that CMOS production past 100-nm ground rules is inevitable, but DRAM producers are more concerned that economics may limit future DRAM generations even before 100 nm is reached. The major companies are predicting that Moore's Law will slow toward 2010, but the reduction in cost per function on the chip will continue at the same rate because of changes in systems design, including self-test and error-tolerant architectures and increased integration levels leading to the system on a chip. The most important driver for new technology is the ability to reduce the cost per function on a chip. Present limitations are cross-talk and the lack of a silicon light emitter to increase functionality. Eventually, RF and optical functions (optical interchip/intersystem and on-chip interconnects) will be integrated onto CMOS/BiCMOS[1] chips to reduce systems costs. MCMs having two- or three-chip solutions instead of a one-chip solution may be a less expensive approach over complete systems-on-a-chip. Figure 8.3-1 is an example of a future system-on-a-chip.

[1] BiCMOS technology is a combination of Bipolar and CMOS technology. CMOS technology offers less power dissipation, smaller noise margins, and higher packing density. Bipolar technology, on the other hand, ensures high switching and input/output (I/O) speed and good noise performance.

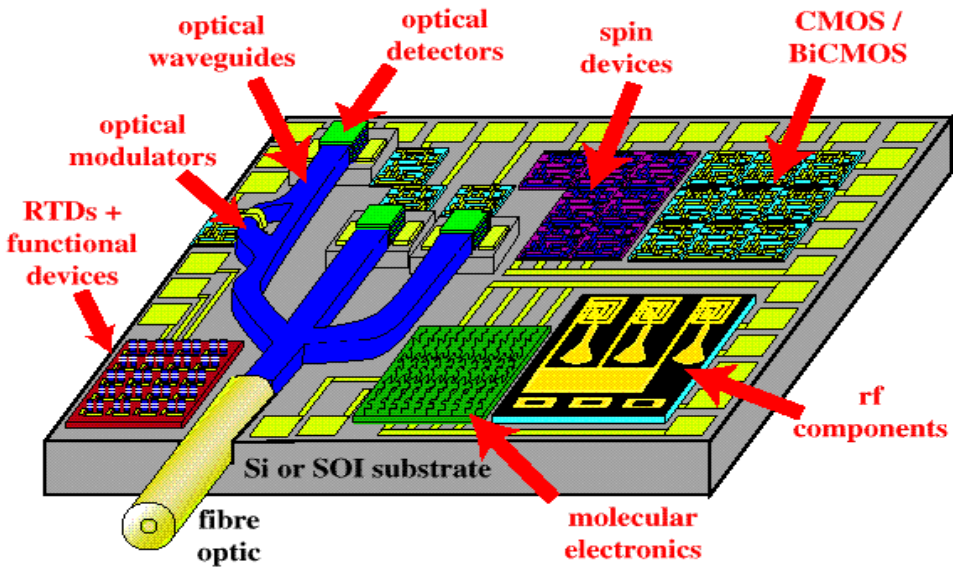

Figure 8.3-1. Future System-on-a-Chip
(Source: ESPRIT – Microelectronics Advanced Research Initiative Nanoelectronics Roadmap)
http://www.cordis.lm/esprit/src/melari.htm

BACKGROUND

Industrial-applicable nanofabrication techniques must be able to produce millions or billions of these small structures in a quick, reliable, and cost-effective way. These techniques must be able to connect these structures in a predefined manner. For this reason, parallel techniques, such as conventional circuit lithography techniques using mask alignment and pattern transfer, seem to be the only currently realistic way to fabricate circuits that are highly integrated. Serial techniques, such as scanning probe techniques or e-beam lithography, may be useful for mask making, or single component fabrication but do not supply adequate throughput for large-scale ICs. Nanotechnology seeks improved speed, density, power, and functionality beyond that achieved by simply scaling transistors.

Indications are that this technology will produce extremely small, very fast computers, integrated sensor applications using terahertz signals, and lightweight compact communication equipment—all with low power consumption.

DATA SHEET 8.3. NEXT-GENERATION LITHOGRAPHY

Developing Critical Technology Parameter	For microelectronics, lithographic technologies for the generation and transfer of highly complex patterns below 100 nm and to extend resolutions to 50 nm, using proximity X-ray, e-beam projection, EBDW, and ion projection [see ***E-Beam Stepper; Background; Lithographic Requirements*** **(Table 8.3-2); and Scattering With Angular Limitation in Projection Electron-beam Lithography *(SCALPEL)***].
Critical Materials	Advanced resist systems (bi-layer, thin-layer imaging, chemically amplified); X-ray, charged beam materials; antireflective materials for X-ray, e-beam, ion beam.
Unique Test, Production, Inspection Equipment	e-beam, X-ray, ion beam exposure equipment; mask inspection equipment; scanning probe microscopy (SPM); scanning capacitance microscopy (SCM); wafer level defect recognition and analysis.
Unique Software	Defect recognition and analysis; OPC; SQC.
Major Commercial Applications	Lithography is used in the fabrication of all semiconductor devices, MEMS devices, and ICs.
Affordability	Not an issue.

BACKGROUND

Lithography is the enabling technology that has supported the IC industry for decades. New, advanced lithographic technologies are required to adhere to the advanced performance projections for IC devices in the 21st century.

Lithographic Requirements

Advanced technologies, such as X-ray and EBDW, have been used to fabricate functional semiconductor devices below 100 nm over small field sizes at low throughput. In addition, various technologies have been proposed and studies are underway to extend resolution to 50 nm. X-ray mask capability for 180-nm generation is in development. Overlay requirements are among the most difficult technical challenges in lithography. Overlay and CD improvements have not kept pace with resolution improvements. The estimates for overlay appear to plateau around 30 nm.

Table 8.3-2 lists projected advances in lithography and overlay. This will be inadequate for ground rules less than 100 nm. Overlay CD control over large field sizes continue to be a major concern for < 130-nm lithography. Advances in stage technologies, environmental controls, interferometers, and alignment systems will be needed for < 65 nm overlay. Continuous improvements in mask-making technology (mask writers, inspection, repair, and substrates) required to support the technical and manufacturing needs of optical lithography below 250 nm. Mask inspection requirements will become more aggressive as X-ray and e-beam lithography push to finer resolutions. In addition, significant improvements will be necessary for all nonoptical approaches, especially 1× proximity X-ray. Major process and materials development is required to achieve the tolerances and mechanical properties necessary in the unique substrates used in these advanced technologies. Key issues will be identifying and repairing defects and the ability to keep masks defect free in manufacturing.

Table 8.3-2. Critical Level Lithography Requirements
(Source: SIA NTRS)

Year of Production	1999	2001	2003	2006	2009	2012
Technology Generation	**180 nm**	**150 nm**	**130 nm**	**100 nm**	**70 nm**	**50 nm**
Product Application						
DRAM (bits)	1G	2G	4G	16G	64G	256G
MPU (logic transistors/cm^2)	6M	10M	18M	39M	84M	180M
ASIC (usable transistors/cm^2)	14M	16M	24M	40M	64M	100M
Minimum Feature Size						
MPU Gates (Isolated lines)	140	120	100	70	50	35
DRAM (Dense lines)	180	150	130	100	70	50
Contacts	200	170	140	110	80	60
Gates (nm, 3 sigma)	14	12	10	7	5	4
Overlay (nm, mean + 3 sigma)	65	55	45	35	25	20
DRAM Chip Size (mm^2)						
Year 1	400	480	560	790	1120	1580
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MPU Chip Size (mm^2)						
Year 1	360	400	430	520	620	750
Year 2	290	240	260	310	370	450
Year 3	220	240	260	310	370	450

Scattering With Angular Limitation in Projection Electron-Beam Lithography (SCALPEL)

SCALPEL is emerging as a viable choice for producing lithography generations below the 180-nm critical dimension. It provides image resolution and fidelity beyond the reasonable diffraction limits of advanced UV optical lithography tools. Wafer throughput will be a major factor in determining which post-optical lithographic technology candidate will provide the best productivity per unit cost. The SIA NTRS illustrates the need for device productivity in the post-optical generations, with increasing wafer size and multiple "shrink generations." In evaluating new lithography approaches, throughput must be normalized to various initial and continuing costs of the tools, masks, resists, metrology techniques, and supporting infrastructure.

In the past, e-beam lithography lacked sufficient throughput to be economically viable for chip manufacturing. In contrast EBDW systems, SCALPEL is a projection imaging system, distinguished by its use of an electron-scattering contrast generation mechanism. Proponents expect SCALPEL to overcome the limitations of optical lithography and enable the migration of chip technology to the 50-nm generation and beyond. An e-beam has a wavelength many times shorter than that of the UV light source used in today's lithography tools and has already demonstrated capability to pattern images well below 100 nm. Electron optics designed for the SCALPEL approach can typically provide a 3-mm wide wafer-scale effective field in which an imaging subfield of 0.25-mm width can be dynamically deflected without mechanical stage motion to expose the 3-mm area. High throughput is enabled by associating mechanical-stage motion in conjunction with the unit area to cover the wafer.

DATA SHEET 8.3. OPTICAL METROLOGY (WAFER INSPECTION)

Developing Critical Technology Parameter	An important area in optical metrology is wafer/mask inspection. The required precision for critical dimensions is in the tens of nanometers for critical dimensions of 250 nm and below. This presents a fundamental challenge and requires research on several fronts. Two approaches to solve this challenge are vector beam imaging and near-field optics. Critical technology parameters are CD measurement precision (5 nm) and minimum detectable particle size (5 nm).
Critical Materials	Materials for ultrasharp metal tip fabrication (near-field optics); bulk material for polarization control and waveguide optics for polarization control.
Unique Test, Production, Inspection Equipment	Near-field optical systems (currently in production but techniques for enhanced sensitivity and resolution are in active development); vector beam imaging (in its infancy and needs considerable research investment); precision mechanical systems for scanning (important in both fields).
Unique Software	High-speed acquisition/processing of digital images.
Major Commercial Applications	Semiconductor inspection; biological imaging.
Affordability	No near-field systems suitable for automated semiconductor inspection are currently available. Laboratory systems are $1–2 K.

BACKGROUND

The use of silicon ICs pervades defense and commercial communication systems and military weapons systems. For ICs to continue to support the current requirements, they must become two to four times more dense in terms of computer power. As line widths and device sizes decrease, critical dimension measurement and particle detection become very critical.

DATA SHEET 8.3. SMALL CRITICAL-DIMENSION LITHOGRAPHY

Developing Critical Technology Parameter	In 10 to 20 years, the applications for microchips will require width or feature dimensions in the 5–10-nm range. Critical-dimension lithography technology requires the UV reflective and transmissive and catadioptic optics to address these wavelengths. Thin-film resist technology for 5–10-nm wavelengths and nonlinear material for super-resolved writing need to be developed. EUV light sources in the 5–10-nm range, in combination with near-field and nonlinear processing technology, will be required to accomplish this task.
Critical Materials	Thin-film resist material.
Unique Test, Production, Inspection Equipment	Mask overlay and alignment to better than 1 nm and defect (amplitude and phase metrology) measurements to 0.2 nm root mean square (rms) must be developed. Advanced aspheric polishing techniques and low-absorption refractory materials will be required. EUV phase-shifting interferometrics to characterize defects clearly is also required.
Unique Software	High-bandwidth schemes for maskless lithography and new considerations for optical design in the X-ray region will be required. Optical component phase measurement algorithms will be needed to characterize defects.
Major Commercial Applications	Many commercial applications (everything from computers to vehicle microprocessors) will benefit from this technology.
Affordability	In the 5–10-nm feature regime, one can fit 3–5 times as many chips on a given semiconductor substrate, thereby significantly reducing the cost of a given chip.

BACKGROUND

This technology will inherently reduce the susceptibility of space electronics to radiation. The smaller features reduce the footprint of the electronics and allow many more algorithms and redundant circuits to fit on the same size chip that is currently used. Many military applications will benefit from this technology, especially since the overall cost will be reduced with the decrease in feature size (thus increasing the yield of chips per substrate). The small patterns are then used in combination with deposition, lift-off, and implantation technology to produce microcircuits on semiconductor chips.

DATA SHEET 8.3. SOFT LITHOGRAPHY FOR MICROELECTROMECHANICAL SYSTEMS (MEMS)

Developing Critical Technology Parameter	Lithographic technologies for the generation and transfer of more complex patterns, for micromechanical structures using EUVL that employ 10–14-nm soft X-ray photons; 193 nm UV lithography; proximity X-ray; e-beam projection; EBDW; ion projection; soft lithography for MEMS.
Critical Materials	Advanced resist systems (bi-layer, thin layer imaging, chemically amplified); X-ray, charged beam; EUV; optical materials; antireflective materials for optical, EUV, X-ray, e-beam, ion beam.
Unique Test, Production, Inspection Equipment	Optical, e-beam, X-ray, ion beam exposure equipment; front and backside mask alignment; mask inspection equipment; SPM; SCM; wafer level defect recognition and analysis; surface proflier; SEM.
Unique Software	Defect recognition and analysis; OPC; SQC.
Major Commercial Applications	Lithography is used in fabricating all MEMS devices. MEMS devices and macro systems will have broad commercial applications ranging from biomedical, diagnostics, automotive, robots, sensors, communications, and aerospace to printers.
Affordability	Lithographic fabrication processes for MEMS must be based on high volume and low cost.

BACKGROUND

Using an ever-expanding set of fabrication processes and materials, MEMS technology will provide parallel micro-assemblies, nonsilicon substrates, and fully 3–D structures, with the advantages of small size, low power, low mass, low cost, and high functionality.

Soft Lithography

Soft lithography refers to a set of low-cost techniques that will expedite the affordability and manufacturability of MEMS devices and systems. This approach relies on elastomeric elements to print organic inks (microcontact printing), to mold polymers (replica molding, micromolding in capillaries, and microtransfer molding), and to perform lithography in the near field. Fabrication of patterns and structures with feature sizes as small as 30 nm on both planar and nonplanar substrates has been demonstrated.

The soft lithography techniques use an elastomeric PDMS element with patterned relief on its surface to generate features. The PDMS elements are prepared by casting prepolymers against masters formed by conventional lithography. The methods can generate features on curved and reflective substrates and can pattern large areas rapidly—both metals and polymers. Distortion currently limits the methods to fabrication of single-layer structures. Near-term applications could include optical devices like polarizers, filters, wire grids, and surface acoustic wave (SAW) devices. Long-term goals include optical data storage systems, FPDs, and quantum devices. Soft lithography is not currently competitive with conventional lithography for multilayer fabrication where there are critical requirements for pattern regularity.

Soft lithography techniques include:

- **Nearfield phase shift lithography.** A PDMS element with micron-scale surface relief in conformal contact with a layer of photoresist modulates the intensity of light in the nearfield region. At phase boundaries, an intensity null results from a p-phase shift between recessed and unrecessed regions. Feature size range is 50–100 nm.

- **Replica molding.** A PDMS element is cast against a conventionally patterned master. Polyurethane is molded against the PDMS secondary master, thus replicating the original without damage. Feature size range is 230 nm.
- **Microcontact printing.** An alkanethiol solution is used to ink a patterned PDMS stamp. The stamp is brought into contact with the substrate, and the thiol ink is transferred and then forms a self-assembled monolayer that acts as a resist to etching. Feature size range is 300 nm.
- **Micromolding in capillaries.** Continuous channels are formed when a PDMS element is brought into conformal contact with a solid substrate. Capillary action fills the channels with a polymer precursor. The polymer is cured, and the stamp is removed. Feature size range is 1 nm.
- **Microtransfer molding.** A PDMS element is filled with a prepolymer or a ceramic precursor and placed on a substrate. The material is cured, and the stamp is removed. Feature size range is > 250-nm multilayer capability.
- **Solvent-assisted microcontact molding.** A PDMS element with a small amount of solvent spread over it is brought into contact with a polymer such as photoresist. The solvent swells the polymer, expanding it to fill the surface relief of the mold. Feature range is 60 nm.

DATA SHEET 8.3. TECHNOLOGY FOR MICROELECTROMECHANICAL SYSTEMS (MEMS)

Developing Critical Technology Parameter	MEMS technology enables the development of chemical, biological, and mechanical smart systems. MEMS is based on a manufacturing technology that has roots in microelectronic fabrication technology. It merges the functions of computing, communication, and power together with sensing, actuating, and control to interact with the physical world.
Critical Materials	Thick photo resist; silicon substrates; SiC substrates; thin-film polysilicon; fluxless solder; piezoelectric thin films.
Unique Test, Production, Inspection Equipment	Front and backside mask alignment; surface proflier; plasma processing (etch and deposition); SEM; cluster tools; MBE; MOCVD.
Unique Software	CAD software for process, system, and packaging simulation.
Major Commercial Applications	MEMS devices and macro systems will have broad commercial applications ranging from biomedical, diagnostics, automotive, robots, sensors, communications, and aerospace to printers.
Affordability	MEMS devices will be a small fraction of the system's cost, size, and weight but will be critical to its operation, reliability, and affordability.

BACKGROUND

Using an ever-expanding set of fabrication processes and materials, MEMS technology will provide parallel microassemblies, nonsilicon substrates, and fully 3–D structures, with the advantages of small size, low power, low mass, low cost, and high functionality. New device concepts include the integration of micro devices with communication, control, computation and power components; miniature electromechanical signal processing elements (tuning elements, antennas, filters, and mixers); miniature optoelectromechanical devices; switches; fiber-optic interconnects and aligners; deformable gratings and tunable interferometers; force/motion balanced accelerometers and pressure sensors; atomic-resolution data storage; process control; and simultaneous, multiparameter sensing with monolithic sensor clusters.

Advanced device and process concepts exploit integrated, collocated actuators, sensors, and electronics to achieve new functionality, increased sensitivity, wider dynamic range, programmable characteristics, designed-in reliability, and self-testing.

SECTION 8.4—MICROELECTRONICS

Highlights

- The 1997 SIA NTRS predicts a very fast-paced growth of semiconductor technologies to the year 2012. Feature sizes of 50–100 nm and densities of 275 Gbits/chip for DRAMs and 1.4 Gbits/chip for microprocessors (108 transistors/cm2) are predicted.
- All the microelectronic characteristics projections are based on current techniques.
- Continual evolution of existing technologies [see Weapons Systems Technologies List (MCTL)] are shown here—from microprocessors, converters, memories, and gate arrays to the evolution of such emerging devices as neural networks, artificial intelligence (AI), optoelectronics, new materials, and advanced packaging.
- Microwave and other RF devices at the IC level are continuing to advance with higher frequency and power, following the rest of the technology but at a slower pace. SiGe, Si, GaAs, InP, and GaN are enhancing this effort.
- Advanced packaging technologies will increase the usability of density, speed, heat control, integration, and environmental technologies, which the extreme densities require.
- Radiation and temperature tolerance are improved by the application of new materials and fabrication.

OVERVIEW

Semiconductor devices are pervasive in all military applications involving electronics. This subsection contains all the digital, analog, and hybrid (analog and digital combined) technology semiconductor devices at the IC level, PCB, or module level. Environmental technology, such as temperature and radiation tolerance, is included for these devices. Also covered are the MMICs and other RF devices operating at higher frequencies and power and not incorporating the emerging applications of SiC and GaN; IC design and testing involving the CAD of chips, PCBs, and modules; and advanced materials and materials techniques, such as SiC and SOI.

Very-high-performance microprocessors of the future will be the main element in supercomputers made of networks of microprocessors. The extreme numbers of elements on a chip will allow an individual microprocessor to be a supercomputer itself, composed of multiple processors networked on the chip along with a very large memory and multiple I/O channels to form very powerful “systolic arrays.”

The integration of electronics and mechanical structures called MEMS will enable complete 3-axis inertial navigation “systems-on-a-chip,” including Global Positioning System (GPS) processing and interface, error modeling, drift compensation, and initialization.

LIST OF TECHNOLOGY DATA SHEETS
8.4. MICROELECTRONICS

DATA SHEET 8.4. ADVANCED PACKAGING OF INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	Next-generation technologies must be developed for high-speed, mixed-signal circuits and increased level of integration, including embedded components and MEMS devices, to achieve functionality and miniaturization.
Critical Materials	High-density interconnect substrates [e.g., those using laminated multi-chip modules (MCM-Ls)], such as flex tape, are primarily multilayer plastic packages made up of copper and epoxy resin, ceramic multi-chip modules (MCM-Cs), deposited thin-film multi-chip modules (MCM-Ds), and built-up multilayer technology, such as MCM-L/D and MCM-C/D for wafer scale processing. For micro-via technology, laser and photo-imageable dielectric layers and plasma etch technology are critical.
Unique Test, Production, Inspection Equipment	Burn-in and test fixtures and testers for MCMs or multi-chip assemblies (MCAs); thermal enclosure/interface systems for control of high temperature during testing; wafer level burn-in and testers for known good die (KGD); interconnects using copper; and optical microscope for solder reflow process control for bumping.
Unique Software	Design tools software; test and analysis software; process control software; thermal management software.
Major Commercial Applications	Solid-state memory; embedded processors for hand-held and portable products, desk-top personal computers (PCs), notebooks, smart cards, camcorders, medical devices, analog/digital wireless applications, high performance computing (HPC) platforms, signal processors, communications, automotive, engine controls, and system-on-a-chip prototypes.
Affordability	In commercial markets, volume is the driver. Electronics-packaging and interconnect technology advances are leading to a small-die-size, ultrathin, lightweight, and low-cost package. CSP (flex tape and flip chip) technology represents only 25 percent of the total IC units assembled (leadframe packages). At present, advanced packaging is 3 times (1.5 cents vs. 0.5 cents/lead) the cost of thin small outline package (TSOP) and shrink small outline package (SSOP). However, with growing applications and existing manufacturing infrastructure, coupled with improvements in substrate materials and processes, it is expected that the prices will be as good or better. Smaller size, lower weight, and higher performance CSP and enhanced CSP packages are much more affordable and provide a better payoff to the system designer.

BACKGROUND

Multichip packages provide higher performance and increased miniaturization over individually packaged devices. Initial applications are in high reliability, high-speed modules, and compact functions. Since the inception of ICs, every improvement has required packaging innovations that do not degrade the IC's performance. Until the last several generations, these improvements have been achieved in a standard way.

Today's and future generations of ICs, with high-speed (gigahertz), high-heat dissipation (up to 50 W), and dense complex structures (gigabytes of memory and 10^{12} logic elements), require new approaches and new technologies. The large heat dissipation requires improved heat transmission from the active elements and the sub-strate. The higher temperature operation requires all the elements of the package to have similar or compensating differential expansion so the structure is not ruptured. Diamond films (and diamond substrates) have superior heat transmission. Copper runs have lower resistance and therefore generate less heat and conduct heat efficiently. Flip-chip and solder-bump connection techniques improve density and connectivity of larger MCMs.

All these technologies must not degrade the performance of high-speed chips at the subsystem interface layer. The MCM technology is a prototype for even denser chips that can incorporate multichips into a single chip as well as become the ultimate system-on-a-chip, which will include MEMS, optoelectronic functions, and hybrid analog and digital circuits.

DATA SHEET 8.4. APPLICATION-SPECIFIC INTEGRATED CIRCUITS (ASICs) [CUSTOM INTEGRATED CIRCUITS (ICs)]

Developing Critical Technology Parameter	By 2012, 100 million gates/cm^2 at 1.5 GHz, with standard cells (microprocessor, memory, hybrid, I/O, A/D, and so forth) integrated into system (system-on-a-chip) ICs. Will perform almost all required applications and be competitive with GPICs. ASICs will be a large part of the future system ICs.
Critical Materials	Wafer flatness; minimum defects; uniformity for advanced ICs.
Unique Test, Production, Inspection Equipment	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment; chip probing.
Unique Software	Standard cell software simulation and modeling; high-level development language (HDL); common application environment (CAE); and automated test equipment (ATE).
Major Commercial Applications	Pervasive to all commercial and military applications. Will compete with GPICs.
Affordability	Developed by commercial.

BACKGROUND

ASICs are "hardwired" (e.g., nonreprogrammable) logic devices that can contain complex logic, memory [DRAM, read-only memory (ROM), electrically erasable programmable read-only memory (EEPROM)], I/O circuits, and so forth—all on a dense chip with a large number of transistors (10^6–10^7 in future). The technology is much like designing a general-purpose microprocessor or other special-purpose processors. Rather than use a programmable system in high-production electronics, a better approach is to fix the complete functionality of the chip (by using programmable devices) in an ASIC. The resulting chip is smaller, more economical, and more reliable than software-programmable devices.

ASICs are generally composites of "cells" transferred from other designs directly, such as logic for a whole microprocessor, a large DRAM and/or programmable read-only memory (PROM) [erasable programmable read-only memory (EPROM) or EEPROM], standard I/O structures for interfaces, timing circuits, and other whole functions desired. ASICs can be hybrid ICs (i.e., a mixture of analog, digital, and conversion functions).

In the future, a large percentage of mass-produced ICs will be ASICs. The ability to design a whole new unique structure using rapid prototyping design techniques (software or firmware) and HDLs can be done economically, fast, and correctly with minimum test time because the individual cells have been used many times and are therefore thoroughly tested and reliable.

ASICs allow the user to use ICs when ordering a standard device is impractical. The specified parameters indicate speed capabilities, which separate these devices from "run-of-the-mill" devices. Most ASICs have resulted from commercial development, but some have originated through military development.

ASICs can be produced in large quantities. They are reliable and are at the lowest cost per unit. Almost any electronic system house can create ASICs.

DATA SHEET 8.4. ARTIFICIAL INTELLIGENCE (AI) AND LEARNING INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	By 2017, 100 million neurons, with self-learning capability artificial neural networks (ANNs). Programmability of ICs for modeling and learning systems.
Critical Materials	Wafer flatness; minimum defects; uniformity for advanced ICs.
Unique Test, Production, Inspection Equipment	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
Unique Software	Training algorithms; simulation algorithms; simulation and modeling; HDL; CAE; ATE.
Major Commercial Applications	Robotics; nonlinear systems; modeling; control systems; central controller for very large systems; air traffic control; power plants; distribution networks; modeling of weather systems and other unpredictable systems.
Affordability	Cost of applying to specific military application.

BACKGROUND

High performance is required in complex control and decision-making systems ("expert or self-learning systems"), parallel processing systems, sonar signal discrimination, and speech and image recognition. Hardware and generic programming technology are available. Overlap between commercial and military applications could be large, allowing compatible usage.

Many countries are interested, and some are conducting R&D. Japan is probably the world leader, with the United States a close second. The United Kingdom and other European countries are also entering this technology field. As soon as much larger ICs are available to provide the working element and the system application has matured somewhat, the worldwide activity will increase in this technology area.

DATA SHEET 8.4. COMPOUND SEMICONDUCTOR INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	Denser ICs to achieve complex functions; matching packaging materials for uniform expansion at high temperatures.
Critical Materials	Compound materials (semiconductor, e.g., III/V and II/VI); GaAs epitaxial wafers; wafer flatness; minimum defects; uniformity for advanced ICs.
Unique Test, Production, Inspection Equipment	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment; chip probing modified for compound materials.
Unique Software	Simulation and modeling; HDL; CAE; ATE.
Major Commercial Applications	Space electronics requiring radiation tolerance; jet engines for wide temperature range.
Affordability	One of the more expensive developments for the military but large payoff for both military and commercial areas.

BACKGROUND

Compound semiconductor ICs have attributes for high-radiation and/or high-temperature usage in a wide range of systems. They can be used to develop the integration of multiple-material ICs and can be used for all electronic equipment requiring unique properties for radiation hardening, wide temperature range, and so forth. Military and commercial areas share much basic research.

Compound semiconductor ICs have not reached their full potential for military applications because of modest volume and infrastructure needs that cannot be satisfied without compromising affordability. They have also not fully met their promise because of difficult materials and fabrication problems. These technologies have not had the large development funding or experience that the silicon ICs have had and are therefore running behind. However, the promise of special operational capabilities (rad-hard, high-temperature) have continued to propel these technologies forward. They will grow in capability as their properties become better understood and as the infrastructure is built to further the technology.

DATA SHEET 8.4. CONVERTER INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	100 MHz to 1 GHz samples/sec; 12- to 20-bit accuracies.
Critical Materials	Wafer flatness, minimum defects, and uniformity for advanced ICs.
Unique Test, Production, Inspection Equipment	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
Unique Software	Simulation and modeling; HDL; CAE; ATE.
Major Commercial Applications	Sensors, inertial guidance and navigation, control systems; display systems; medical systems.
Affordability	Not determined.

BACKGROUND

These Converter Integrated Circuits are immediately available from commercial output. Overlap between commercial and military application could be large, allowing compatible usage.

DATA SHEET 8.4. EXTREME ENVIRONMENT INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	Radiation > 5×10^6 rads (Si); total-dose-five merging devices; jet engine and automobile controls to 400 °C.
Critical Materials	Wafer flatness, thickness, defects, and uniformity for advanced ICs; ceramic, metal ceramic, diamond substrates, and diamond coatings; uniform expansion/contraction developed to mitigate thermal shock; SOI wafers; dielectric materials.
Unique Test, Production, Inspection Equipment	Dielectric isolation; SIMOX ion-implanter for deep implant on silicon-on-sapphire (SOS) and SOI; controlled doping; MBE; surface passivation; controlled radiation testing; reliability and failure analysis.
Unique Software	Computer modeling and simulation software; pre- and post-radiation modeling; SEU models; thermal analysis models; diagnostics for modeling of starting materials.
Major Commercial Applications	All future large, low-power, high-speed, and high-density ICs as nanoelectronics are approached; commercial communications satellites; jet engines.
Affordability	Future commercial ICs in military systems will be more usable by COTS materials if military specifications are not too stringent. For military rad-hard devices, cost is an issue because of unique rad-hard-specific processes and low-volume requirements.

BACKGROUND

The ability of ICs to withstand the extreme environments of radiation, temperature, shock, and vibration improves the probability of reliable operation for all space-based systems. Generally, “mid-temperature range” has been accepted as an indication of improved long-term reliability for commercial systems, but the capability to operate at specified temperature extremes is critical in certain applications (e.g., missiles and nuclear systems) and may require special processing and packaging.

Commercial IC capabilities are continuously evolving to keep pace with the SIA NTRS. New technologies (e.g., SOI and SiGe wafers with Cu and low-k dielectric interconnects) are being implemented for low-power and high-speed complex ASICs, memory, and processors. However, the rad-hard-specific CMOS/SOI process and technologies are two to three generations behind the commercial IC device development and manufacturing.

As the COTS products become more common in the DoD environment, system designers can take advantage of the commercial capabilities and, by making modifications to the existing process and packaging techniques, develop systems to meet the radiation-tolerant applications for future military systems. However, for more stringent rad-hard and extreme-temperature devices, special circuit design/modeling, materials, and process development efforts are needed to keep pace with the commercial capabilities.

DATA SHEET 8.4. FIELD-PROGRAMMABLE INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	Merging gate arrays and logic arrays into best architecture for field-programmable ICs; very large devices for all ranges of applications (especially ASICs); 1 million usable gates by 2012.
Critical Materials	Wafer flatness, minimum defects, and uniformity for advanced ICs.
Unique Test, Production, Inspection Equipment	Lithography, epitaxy, deposition masks, and resist for high-density chips; high-speed testing equipment.
Unique Software	Standard cell software simulation and modeling; HDL; CAE; ATE.
Major Commercial Applications	Same as all future applications competing with GPICs.
Affordability	Commercially developed.

BACKGROUND

Field-programmable ICs will be used to prototype, modify, and upgrade military systems such as avionics, computers, radar, and guidance systems. Field-programmable gate array devices allow on-field changes to be made to existing firmware or software because of software changes, database changes, or additions to firmware or software.

A prime commercial use of field-programmable ICs is for programming a system temporarily for field test (e.g., Beta Site) before finalizing production design. These devices can be compatible or interchangeable between commercial and military systems.

Field-programmable ICs are available from the commercial sector.

DATA SHEET 8.4. MEMORY INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	Very large (256 GB) memory ICs (DRAM, SRAM, EPROM, EEPROM); large memory cells to be integrated into general-purpose microprocessors or ASICs by 2012.
Critical Materials	Wafer flatness, minimum defects, and uniformity for advanced ICs; GaAs, SiC/compound semiconductors.
Unique Test, Production, Inspection Equipment	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
Unique Software	Standard cell software; simulation and modeling; HDL; CAE; ATE.
Major Commercial Applications	Pervasive to all commercial and military electronic systems.
Affordability	Commercial development will supply almost all military requirements if COTS products can be used or the commercial output can be directly converted to MIL-SPEC devices.

BACKGROUND

It is expected that memory devices, like all ICs that follow "Moore's Law," will advance to the next generation every 2–3 years. The only constraint is the ability to invest large sums of money (approaching $1 billion in the future) for the highly complex fabrication equipment that also must evolve in the same fashion. Certainly, gigabytes of memory on a chip will be available in several generations.

Further in the future, the role of memory in ASICs will begin to replace general-purpose microprocessors in many applications (not considering PCs, workstations, and so forth). Although ASICs for special-purpose functions in electronic systems are becoming very large and complex, they are easy to design and produce. So, the large bulk of future ICs will be for special-purpose functions with all firmware and databases stored in memory driven by a simple controller and complex interfaces.

DATA SHEET 8.4. MICROPROCESSOR INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	System-on-a-chip, including MEMS and optoelectronics; megabytes of SRAM on chips by 2012 for program and cache memory; 10-GHz speed by 2012; 1.4-B transistors/chip, including SRAM.
Critical Materials	Wafer flatness, minimum defects, and uniformity for advanced ICs; diamond substrates and coatings; efficient interconnects (such as copper).
Unique Test, Production, Inspection Equipment	Lithography, epitaxy, deposition masks, and resists for high-density chips; high-speed testing equipment.
Unique Software	Simulation and modeling for complex systems; HDL; CAE; ATE.
Major Commercial Applications	Virtually all commercial applications; digital signal processors (DSPs); systolic arrays; massively parallel systems.
Affordability	Commercial (free) development allows direct use by military. Additional cost is incurred if military must meet MIL-SPEC requirements.

BACKGROUND

Microprocessor ICs have become necessary and critical components in military and commercial systems.

The family of microprocessors includes single chips and software programmable, factory-programmed, or field-programmable devices. In all these cases. the processor can perform a wide range of operations (e.g., acting as digital filters of all types and controllers or as general-purpose processors for system control, analysis, or computational functions). All these operations are equally useful in military or commercial applications.

The primary developers of microprocessor ICs are commercial IC companies since the applications in the commercial sector develop much faster than applications in the military sector. The commercial market demands new generations of ICs every 2–3 years, whereas inserting new or developed products into military systems can take 8–10 years.

DATA SHEET 8.4. SYSTEM-ON-A-CHIP INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	Integrate electronics, MEMS, optoelectronic, and hybrid circuits on a single chip, with all appropriate interfaces and A/D and D/A conversion.
Critical Materials	None identified, other than those noted on other data sheets.
Unique Test, Production, Inspection Equipment	Probe testing; total system testing; partial chip testing; ability to fabricate all these dissimilar technologies on a chip.
Unique Software	Simulation and modeling, including electronic, mechanical, optical; HDL.
Major Commercial Applications	Navigation and guidance; sensors; effectors; medical testing; miniature systems needing all characteristics.
Affordability	Design and fabrication cost will be high. Sufficient production will be required to justify cost.

BACKGROUND

Initial efforts will take advantage of extreme functional density to fabricate all electronics, including general-purpose computers (GPCs), DSPs, hybrid electronics, memory, and interface electronics for a large system function. Additional efforts will include integration of these same technologies, combined with MEMS, to develop gyros, accelerometers, medical sensors, and any miniature electromechanical functions. Electronic and optoelectronic integration will improve the development of computers, digital filters, and other signal-processing functions. The eventual goal will be to integrate all these functions into a single chip.

This technology is in its infancy and has not yet taken advantage of the extreme functional size of even today's ICs. Some work has been done to put electronic interfaces on a MEMS accelerometer and gyroscope to create a workable function to interface with other navigation and guidance functions. Since MEMS are fabricated by IC equipment at micron-size features, the technology must be pushed to submicron features to be more compatible with today's dense chips.

Many sources are conducting exploratory R&D. Medical in-body sensors may drive the technology to new heights. Satellite navigation and guidance requiring the smallest size will also drive the technology.

SECTION 8.5—NANOELECTRONICS

Highlights

- All the attributes of microelectronics (see subsection 8.4) are further enhanced by entering the nanoelectronics feature size range.
- EUV, X-ray, or ion-projection lithography will be used to break through the 100-nm barrier to achieve feature sizes down to 10 nm.
- The extreme density and speed of nanoelectronic devices will enable "supercomputers on a chip." Integrated optical, mechanical, and electronic "systems on-a-chip," such as complete inertial navigation systems, will be possible.
- Nanoelectronics will enable very small, low power, low cost, sophisticated space probes; microminiature biological probes for the human body; and battlefield surveillance using very small unmanned flying vehicles.

OVERVIEW

Nanoelectronics can be broadly defined as those developing technologies required to push the size of devices down into the 100–10-nm (0.1–0.01 μm) region initially and then into the 10–1-nm region. Today's advances in microelectronics technology continue to shrink the feature size of Si-based FETs and is projected to be 100 nm (0.1 μm) somewhere between 2003 and 2005 or earlier as per the SIA NTRS.

A nanometer is a billionth of a meter—about the size of two large atoms—approximately ten atomic diameters. As this feature size shrinks below 100 nm, it will be more difficult and costly to fabricate these devices. Some investigators even question their functional effectiveness below 70 nm (by the year-2010 SIA NTRS) in ultradense ICs. A 25-nm dimension has been demonstrated, but many technical problems must be overcome before production can be achieved. In addition, packaging, interconnects, and heat will exacerbate the problem. In fact, these problems may be the initial stumbling block as current efforts approach the 100-nm region. Research has been ongoing for approximately the past 40 years to explore the alternatives for nanometer-scale electronic devices that can perform both as switches and amplifiers, just like today's transistors for supercomputing applications. The operating principle for FET is the movement of mass electrons in bulk silicon. In the nanoelectronic world, atoms and molecules rule, and devices take advantage of quantum mechanical phenomenon including the discreteness of electrons.

Molecular electronics is a relatively new approach that would change the operating principle and the materials used in the electronic devices. It uses, primarily, covalently bonded molecular structures, electrically isolated from a bulk substrate. The molecules are naturally occurring nanometer-scale structures and can be made exactly the same by the millions and trillions easily and at low cost for the industrial scale nanostructures needed for the ultradense nanocomputers, where as it is difficult and expensive to fabricate millions and billions of nearly identical nanometer-scale structures in solids. Working at the molecular level could also lead to huge advances in optical communications and photonics, as well as ways to probe individual cells (speculative for now). In recent years, researchers have, for the first time, put together molecular electronics devices that measure only a few nanometers and are viable and inexpensive. Among the molecular switching device categories, the electric-field-controlled molecular devices and electromechanical molecular switching devices are promising because they descend from the solid-state microelectronics and nanoelectronic devices and show promise for super dense integration and super fast computing.

The breakthroughs required for extreme miniaturization fall into the following categories:

- ***Device science.*** Research on molecular electronics has been made feasible and important by the inventions of the new exciting methods called "mechanosysthesis" and "chemosynthesis." Mechanosynthesis is the fabrication of nanostructures, molecule by molecule, using nanoprobes such as the scanning tunneling

microscope (STM), atomic force microscope (AFM), and the new MEMS chips that contain arrays of these STMs and AFMs.

Chemosynthesis is the fabrication of chemical "sub-assembly" of nanostructures using methods available from biochemistry, molecular genetics, and the organic synthesis of molecular electronic devices in individual organic molecules. It takes advantage of the driving force and speed of bulk chemical processes to make great quantities of nanometer-scale structures, such as molecular switches, nanowires, and self-assembled mono layers.

A new device science is required other than the bulk-effect FET. A potential new device might take advantage of quantum mechanical phenomenon that operate at these small feature sizes, including single electron actions. Two such classes are:

- *Solid-state quantum-effect and single electron devices.* This approach takes advantage of the long years of experience on semiconductor transistors.
- *Molecular electronic devices*. This approach is inherently nanometer in scale as it is molecular in nature. However, it requires new materials and processes.

- ***Packaging.*** Packaging for the nanometer-level devices will require extending the known approaches, and inventing completely new approaches, to overcome several difficult problems:
  - Heat dissipation reduction and control
  - Improved interconnects
  - Vertical integration of gate structures
  - 3–D packaging using vertical interconnects
  - New parallel architectures to optimize the chip layout.

  Substrates and MCMs will have to use diamond coatings and metal ceramic technologies to achieve the required cooling. Copper runs (using Damascene and double Damascene techniques) and low-K insulators to achieve the desired speed and cooling will be required, as well as yet unknown techniques.

  The kinds of challenges that need to be addressed are type of interconnection or linkage between molecules and small devices and solid substrate; electromigration and cross-talk problems in thin wires in ultradense structures; redundancy for error correction and reliability; heat dissipation; and the problem of how to arrange enormous numbers (between 10^9 and 10^{12}) of individual devices ultradensely and ultraprecisely on a surface or in a lattice structure. Also, the production of molecules that exhibit requisite electronic effect (e.g., Coulomb blockade) has to be shown.

BACKGROUND

For Moore's Law (double chip density and speed every 18 months) to continue in force, the feature size of semiconductor devices must continue to shrink below 0.10 µm (100 nm) somewhere near the limit of optical lithography. These feature sizes are required for the destiny of chips to achieve the ultimate size required to build very large electronic "systems-on-a-chip." These densities will also allow the integration of optical (both analog and digital), MEMS, and digital and analog electronics on a chip. The applications for chips of these sizes, both commercial and military, will be innumerable.

LIST OF TECHNOLOGY DATA SHEETS
8.5. NANOELECTRONICS

DATA SHEET 8.5. MOLECULAR ELECTRONICS

Developing Critical Technology Parameter	Molecular electronic technology (MET) includes devices relying on the electronic properties of molecules that may contain more than one electron and are not only "single" electron in nature. MET includes "single" electron (quantum cascade or quantum dot) or relies on electron spin. An example is the use of the position or spins of single electrons as the bistable logic gate in implementing nanometer-scale devices (below 10 nm). Microelectronic devices use silicon semiconductor current switching to accomplish bistable elements, whereas MET uses the location of single electrons or their spins as the switching element. The applications of nanometer devices will ultimately improve greatly in performance, size, weight, power, heat dissipation, and perhaps radiation tolerance.
Critical Materials	Spin-controlled materials called magnetic semiconductors or multilayers of these materials have potential for these applications. Semiconductors and metals differ in the number of charge carriers involved. There are too many electronics in metals to be controlled. In semiconductors, the resistivity can be controlled by controlling the number of carriers, as in electrons or "holes." Merging semiconductor and magnetic properties in a single material has been ongoing research for decades. II-VI alloys of magnetic and semiconductor materials are called diluted magnetic semiconductors (DMSs). Bulk forms of these II-VI DMS materials, thin films of III-V DMS (In,Mn)As, and a ferromagnetic DMS (GA,NM)As are the various combinations.
Unique Test, Production, Inspection Equipment	A family of new test, production, and inspection (T, P, and I) equipment comparable to that used in microelectronics will have to be developed. It is not clear how many of the existing techniques can be transferred to nanoelectronics.
Unique Software	Since software is generally independent of hardware, chip tests and systems test for microelectronics might be adapted to nanoelectronics requirements. Testing and inspection during nanoelectronics production will require a completely new set of software. Application software generally should be interchangeable.
Major Commercial Applications	All the same applications used in microelectronics can be used in nanoelectronics. The major emphasis is on applications in which extremely small size, weight, power, and heat dissipation are essential, such as "wearable" electronics (both commercial and military); remote sensor systems (e.g., satellites, space probes, and biological in-body); ultrasmall, remotely piloted vehicles (e.g., microvehicles); and other smart vehicles (e.g., those used for underwater exploration).
Affordability	The initial discovery of the physics of silicon semiconductors has encompassed over 40 years of development and billions of dollars in expenditures. The development of MET has barely entered this kind of cycle. Certainly, initial discovery and analysis of molecular phenomenon has taken place during the last several decades, but the total thrust of development has been for silicon semiconductors. However, industry consensus is that silicon semiconductor technology cannot continue below 100–50 nm. All the technologies required for entering this regime—materials, lithography, deposition, production equipment, testing methodology, equipment, and so forth—must be redeveloped. Certainly, the large, highly trained work force developed during the last five decades can collapse the timetable to achieve practical devices. So the final analysis is the cost to enter this technology. The cost to industry will be even higher because the two paths will inevitably be followed simultaneously—driving the present silicon technology to its ultimate limit and entering the new MET arena with all its uncertainties. History tells us that technologies tend to continue to proceed past their predicted limits. Surely, this will be the case with silicon technology since optical lithography has already exceeded recent predictions.

BACKGROUND

The commercial and military market will pressure electronics to continue to follow Moore's Law (double density every 18 months) and supply ever-higher performance. A challenge is whether the cost will be prohibitive and the users will be trained to accept a slower growth curve. However, the users can be expected to expand their system requirements, particularly with system-on-a-chip. The integration of digital and analog electronics, MEMS, and optoelectronics on a single chip will need ever smaller, lighter, lower power, higher performance, and rugged electronics. In the end, this will determine if the best in silicon technology is good enough to meet all market requirements.

The development of these devices cannot take advantage of all the microelectronic design, production, and application knowledge developed during the past few decades. The silicon technology of the past has become embedded in the culture, and this evolution has allowed tremendous advances to be achieved. However, MET will be a departure from all these existing technology and will require new physics, design, and production technology to be developed at great cost and over a long period of time. The question is, will industry pay the price? Simpler departures in the past have not made the grade (two terminal devices comes to mind).

However, literature search shows that progress is being made in harnessing the principles of quantum mechanics to design and build molecular devices that can function well in nanoscale even after miniaturization of solid-state FETs has ceased to be feasible and cost effective. Before the nanofabrication methods become feasible, the industry may leverage the present microelectronics technology developments to pursue a hybrid solution for aggressive miniaturization by employing quantum effect and bulk devices. This may increase the logic density by as much as 100 or 1,000 times as that presently feasible.

DATA SHEET 8.5. SILICON-BASED INTEGRATED CIRCUITS (ICs)

Developing Critical Technology Parameter	Since industry has continued to invest in time and money in silicon-based semiconductors, it is locked into pushing the technology as far as it will go. It appears that the market will be satisfied for most of the next decade with predictable (some risk and large dollar investments) improvements in the ability of the underlying technologies to design and produce the required ICs into the less than 100-nm range. This is by no means a certainty since fundamental limits not approached to date will certainly at some point come into effect. Optical lithography may allow producing chips down to 50 nm in feature size, but this is not a certainty because of the need for extreme defect-free substrates and other fundamental problems. SIA NTRS projections for 2012 are: • Memory (DRAM) to 200×10^{11} bits/cm^2 • Microprocessor (MPU) to 10^8 bits/cm^2. Present capability is approaching 130 nm in production.
Critical Materials	Low-k dielectric deposition, copper chemical-mechanical planarization (CMP), and SiO_2 gates to achieve low delays (speed > 2 GHz by 2012). For silicon nanodevices, defect-free and flat wafer, thin epitaxial Si or SiGe deposited films, new resist materials and light-sensitive coatings, low-k dielectric deposition, and interconnect materials (e.g., Cu) are critical. For Si nanoelectronic devices growth, and uniformity of SiO_2 to 5-nm thickness as a natural insulating barrier is important. Materials with low defect size, resists compatible with EUVL (see subsection 8.3); heat sinking materials and techniques, such as diamond films, to allow 175 W per chip.
Unique Test, Production, Inspection Equipment	The existing T, P, and I equipment has kept pace with development to allow good ICs to be produced. For the next generation of ICs, this equipment is expected to continue to evolve. The T, P, and I parameters must always be better than the product to test properly beyond the product specifications. This means gigahertz frequencies and nanometer size. For scale-down field tests, development of lithography tools, masks, CMP tools, epitaxy and etch tools, and in-line automated defect inspection equipment with programs to analyze and categorize defects are needed for production. Also needed are ATE that has built-in test and advanced ATE that uses better probes and handling capabilities. The T, P, and I technology is pressed to the limits. A technique to help this situation is placing a permanent built-in test in the chip. Since future chips will have 10 power gates, these chips will have excess real estate available for redundancy, duplication, parallel data paths, stored test software and data, and so forth. This will be true for chip and chip-aided system tests.
Unique Software	New, extensive simulation and modeling capability; HDL, CAE, and ATE; defect monitor and failure analysis software programs for the in-line test. However, this should be an extension of the existing technology. The CAD software must be sophisticated to handle extremely large systems-on-a-chip, which entails analog, digital, optical, and mechanical engineering.

Major Commercial Applications	All the major commercial applications stated in subsection 8.4 apply here, except that the extremely large chips produced at the 50-nm feature size will be system-on-a-chip ASICs and very large computers on a chip (does not seem right to call them microprocessors anymore). These chips will likely be micro-optics-electro-mechanical systems (MOEMS) to take advantage of the large amount of space on the chip not needed for electronics alone. Since there will be a large availability of low cost yet capable chips at large feature size (e.g., in the 100 or less nanometer range), the use of these denser and more expensive chips may need to find their own market niches—in areas such as telecommunications, aircraft, and missiles using small inertial devices; supercomputing; optical communications; and photonics that are expected to be in large systems-on-a-chip.
Affordability	The SIA NTRS projects that the cost of new fabrications will increase to $5 billion over the first decade of this century. The semiconductor industry has been meeting these costs as the new technology and the market demands. To date, the market has increased to absorb the costs and leave the industry profitable. New companies and consortiums have appeared to continue to provide the required output. However, as we approach the physical limits to the technology (projected in 2012 to 2014 at about 50 nm), the incremental costs will grow as elements of the technology become more difficult. Researchers project that to go beyond 50-nm device feature size, the Si FETs may be too expensive and inefficient—and thus unaffordable. At this point, the industry must shift to a new technology ("the new paradigm") to continue the improvement in the product. The previous data sheet, Molecular Electronics, describes this new technology. It is not certain how the industry will absorb the costs of a new technology while in the midst of the most expensive part of the old technology. Since the market will not wait, the two technologies (old and new) must be pursued simultaneously so the transition is seamless.

BACKGROUND

The SIA NTRS "predicts" continual growth to the year 2014, following Moore's Law (double density every 18 months). To continue the march of aggressive miniaturization per Moore's Law and fabricate nanoscale (70 nm to > 5 nm) devices, optical lithography as we know it today will have reached its physical limit by year 2005 and will require new generation of lithography tools/technology to cross the barrier. Next-generation lithography (NGL) technologies, such as EUV using soft X-rays (being developed by an Intel consortium) and SCALPEL using electron-beam lithography, are the prime considerations by SEMATECH/SIA member company experts. IBM's candidate—X-ray lithography—is also in the race. The future cost of new facility using such new tools could run as high as $3 to $5 billion, excluding the cost of development.

Shrinking microelectronics have driven the exponential growth of Silicon Valley, but that growth will stop unless nanoscale computer chips can be fabricated. To continue this trend of miniaturization, the SIA NTRS projects that feature size to shrink to 100 nm by year 2005 (memory) and allows Moore's Law to be in force. Researchers have projected that semiconductor transistors beyond 100 nm may not function as well. The problem is that dominant technology used to make chips. Optical lithography uses light whose wavelength may be too large to do the job. However, it has been shown recently that using phase shift masks and Numeri software techniques may extend optical lithography to 70 nm.